Global Journal of Technology and Optimization

Sandhya, Global J Technol Optim 2018, 9:2
DOI: 10.4172/2332-2543.1000225

Review Article Open Access

Reduced Encoding Complexity for LDPC Codes Using Partially Random and Involutory Matrix Concept in the Generation of Parity Check Matrix

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Received date: May 07, 2018**; Accepted date:** June 14, 2018; **Published date:** June 30, 2018

Abstract

Error correcting codes principally employed in terrestrial video broadcasting technologies are turbo codes. Now-a-days these were replaced by LDPC codes due to low decoding complexity and parallel design, however Turbo codes use serial design that leads to low speed. Besides its advantages, encoding complexity remains a comparatively intensive idea that this remains an open problem. To reduce encoding complexity we proposed a new algorithm. By generating the A square matrix, that is an involutary matrix in parity check matrix H=[A∶B]_(M×N) ends up in complete elimination of inverse matrix, and in turn reduced encoding architecture and area however with lesser girth. The proposed work suits well for applications with moderate performance and was implemented on Virtex 5 kit.

Keywords: Low Density Parity check (LDPC); Encoding complexity; Turbo codes; Involutory Matrix; Matrix inverse

Introduction

The exigency for reliable digital data transmission throughout a real world network is more challenging than ever, that created a demand for higher correcting codes. In digital wireless system, data gets corrupted because of channel interference that is random in nature [1]. So, high performance error correcting codes are needed. Compound codes like LDPC codes and Turbo codes have performance nearer to the theoretical value, thus can be used in digital communication systems. Performance isn't solely the sufficient criteria to define the use of an error correcting code, but they also should be pliable, low complex and low cost to implement etc., are needed. Turbo codes are bitter, complex compared to LDPC codes, this leaded usage of LDPC codes in new generation technologies of terrestrial video television broadcasting standards and WiMax and so on [2-4].

In storage applications and error correcting memory, error correcting codes with moderate performance is sufficient, because internal interference due to the electronic device, thermal noise and so on causes interference, but area, latency and cost are more important as they are the critical parameters while designing the RAM's and ROM's. LDPC with a hard decision decoding algorithms, which are simple to implement can be used in error correcting memory.

Prior to 1990's, LDPC codes were neglected due to its extreme complexity. Later, in the 1990's after its rediscovery with the help of tanner graph, lead to great reduction in complexity. Subsequently, LDPC codes defeated the six turbo codes and convolution codes by replacing them as error correcting code in the DVB-S2 standard for terrestrial video broadcasting and as the forward error correction system for the ITU-T G hn. standard respectively and also became a part of Wi-Fi 802.11 standard [3].

Parity check matrix generation, encoder and decoder are three major blocks of LDPC codes. In recent years, research is mainly focused on the way of reducing decoder complexity and high performance parity check matrix generation algorithms. Different decoder algorithms where developed and are categorized into soft decoding and hard decoding algorithms.

Message passing (MP) algorithm, sum product (SPA) algorithm, min sum (MS) algorithm, extended minimum sum (EMS) algorithms and Min-Max algorithm etc., are soft decoding algorithms. Bit flipping and its variants are hard decoding algorithms. Progressive edge growth and its variants (Modified Progressive Edge Growth etc) are randomly constructed codes which generates short block length codes. Less focused research area is to reduce encoding complexity [1].

Involutory matrix Generation depends on the size of the matrix, check degree sequence and data node sequence. In this paper a new algorithm for generating involutory matrix which is very simple, easy and very low complex is proposed. It's architecture consists of one up/down counter, one up counter, two n bit multiplexer, few comparators and few extra basic gates [5-7]. Based on symbol size (k), row degree sequence (CNS), check node degree sequence (VSN) following cases exits:

Case 1:

This case doesn't exist because rate of the code is less than 0.5 and parity bits are more than message bits which leads to high overhead which is not desirable [8].

Case 2: (Regular LDPC codes)

In this case, checknode's degree and variable node's degree are uniform. Generally check the node degree is odd and mostly it is 3.

Because of low density of 1's in parity check matrix, there exists more than one involutory matrices, and one of them is symmetric matrix and remaining are non-symmetric matrices.

Generally, all symmetric matrices are involutory matrices (even check the node degree fails).

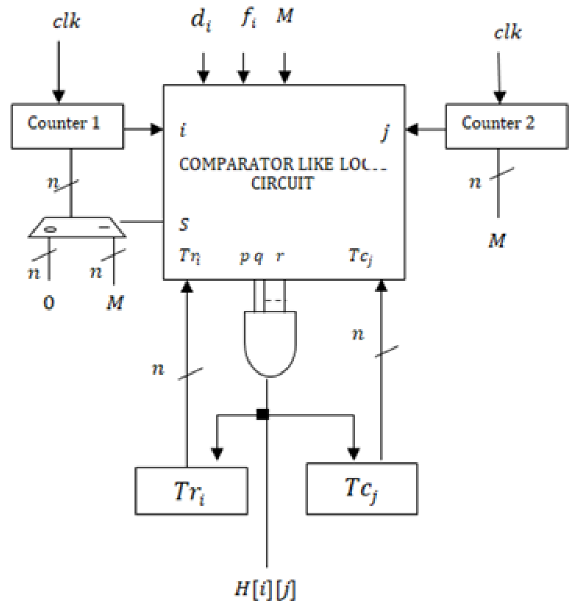

Figure 1: Proposed architecture for Generating A matrix.

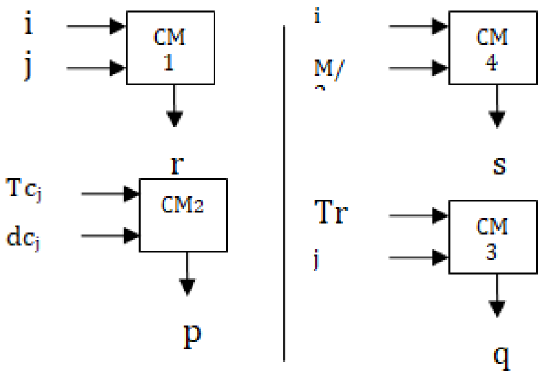

Figure 2: Comparator like architecture symmetrical matrix A generation.

Symmetric matrix generator

For a particular size, check node degree and data node degree there exists only one symmetric matrix. Matrix construction begins with diagonally 1's matrix and & are as per step 2 in algorithm [9]. Now Symmetric matrix is generated by splitting matrix into and matrices with equal sizes. First matrix's construction begins and entry of 1's begins from last row (higher positioned check nodes) towards first row by satisfying the rules in each column starting from the first column. Similarly second matrix is constructed but entry of 1's begins from first row onwards by satisfying the rules 1&2.

Non Symmetric involutory matrix generation

Construction of non symmetric matrix is also similar which begins with diagonally 1's matrix, but size of A1 m1*M and A2 m2*M are different (m1 + m2 = M).

When m1≥2: A1, similar to symmetric matrix, but in matrix the entry of 1 in the last two rows should not begin from second two rows. Further constrained that not more than two rows begin with same positioned row, so that for the sake of uniform distribution [10].

B Matrix Construction

The resultants check node degrees and variable nodes degree sequence's of matrix are irregular. Even structured codes or other random codes can be used to improve girth. When random codes are used to construct matrix then parity check matrix construction was partially random [2]. As matrix having the girth 4, average girth can be increased by constructing the B matrix with higher cycles. Progressive edge growth algorithm offers high girth compared to other algorithms.

Architecture for proposed algorithm for generating A matrix

A novel architecture as shown in Figure 1 was proposed which is very simple to implement, which consumes less area and time. Proposed architecture consists of two counters, some comparator like structure, and few basic gates and few multiplexers. Counter 1 and Counter 2 generates the row and column indices respectively [11]. Matrix generation is a sequential process in each clock cycle only one matrix element will be set to either 1 or 0 based on the outputs of the comparator like structure. Matrix A2 construction was followed by A1 matrix construction. Starting it is equal to 1, then starting load value of counter 1 is , counter 1 and counter 2 output values are M and 0 (couter2 is up counter initially starting from 0) respectively, and from Figure 2 p, q and r 1's for the particular i=M and j=0, then H[i][j] is 1. Comparator like structure is constructed based on the desired structure. Figure 2 shows the comparator -like structure for symmetrical construction, it may vary for non symmetrical construction, and some comparators may be added for the desired structure.

Counter 1

Counter 1 is an up/down counter. It performs counting based on the load value if it is to equal to then it performs down counting otherwise if it is 0, then it performs up counting. The load value depends on the column size of A1 and A2 matrix. For example consider A1 column size 2 then first load value will be 0, and counting begins and once counts reaches to maximum value, then only new load value will be loaded into the counter. In the above considered above example upto three times the load value will be 0.

Counter 2

Counter 2 is a simple up counter with load value always equal to 1. Its count value will be increment after M couter1 cycles. Its count value indicates the column of the matrix.

B Matrix Construction

B matrix can be constructed by using PEG and Mackay's algorithm. Proposed architecture suits for generating it, by design some comparator like structure according to the requirements.

Performance Analysis

Code rate

When code rate is ½ then half of the variable nodes are having girth 4. We can lower these numbers by increasing the code rate. Thus, if the higher the code rate then higher the performance. Thus, proposed work mostly applies for the higher code rate.

Encoder complexity

Encoder complexity is greatly reduced and it depends upon only on the matrix multiplication. The encoding complexity of the Richardson work was shown in Table 1.

N	M	R	Check nodes degree sequence	Variable node check node degree sequence
10	5	0.5	{5,5,5,5,5},{3,4,5,6,6,6},{4,4,5,5,6,6),{3,5,5,5 ,6,6}	{2,2,3,3,3,3,3,3,4,4}
10	5	0.5	{5,5,5,5,5},{3,4,5,6,6,6},{4,4,5,5,6,6),{3,5,5,5 ,6,6}	{1,2,2,3,3,3,3,4,4,5}
10	5	0.5	{5,5,5,5,5},{3,4,5,6,6,6},{4,4,5,5,6,6),{3,5,5,5 ,6,6}	{1,1,1,3,3,3,3,5,5,5}
10	4	0.4	{5,5,5,5,5},{3,4,5,6,6,6},{4,4,5,5,6,6),{3,5,5,5 ,6,6}	{2,2,3,3,3,3,3,3,4,4},{1,2,2,3,3,3,3,4,4,5},{1,1,1,3,3,3,3,5,5,5}, {2,2,2,3,3,3,3,4,4,4,4},{1,2,2,2,3,3,4,4,4,5}
10	3	0.4	{5,5,5,5,5},{3,4,5,6,6,6},{4,4,5,5,6,6),{3,5,5,5 ,6,6}	{2,2,3,3,3,3,3,3,4,4},{1,2,2,3,3,3,3,4,4,5},{1,1,1,3,3,3,3,5,5,5}, {2,2,2,3,3,3,3,4,4,4,4},{1,2,2,2,3,3,4,4,4,5},{2,2,2,3,3,3,34,4,4}

Table 1: Possible check node degree and variable node degree sequences for N=10.

From table we can observe that Richardson encoder consists of six multiplication operations and three matrix addition operations, but in proposed work consists of only two matrix multiplication operations only. But from Table 1 we can observe that encoder complexity was the quadratic effect of g and this effect was completely eliminated in the proposed work.

Decoder complexity

Decoder interconnection complexity of the proposed algorithm a bitter lesser than progressive edge growth algorithm or Mackay's construction because A matrix is Constructed with fixed pattern.

Simulation Results

Implemented the proposed architecture on Virtex 5 and Language used is Verilog HDL while implementing a few counters are added to count the intermediate check nodes and variable node's degree.

Delay

The delay of proposed architecture complete depends upon counter 1 cycle and the frequency. So the total delay to produce the final matrix output is as below

tdelay=(N×M)T

tdelay=(N×M)T tdelay=(N×M)/F

Where, and denotes counter1 clock cycles time period and frequency respectively.

Conclusions

Low encoding complexity is necessary for wireless systems. The proposed work reduces the encoding complexity, but due to girth 4 performance degrades comparatively. But average girth can be increased by using a PEG algorithm for the construction of the matrix B. Generally PEG algorithms offer high girth for higher codeword lengths. This algorithm is best suitable for higher rate codes and performance equals to the PEG algorithm. Storage application requires moderate performance compared to wireless systems, so proposed architecture best suits. From the simulation results it can be observed that construction complexity is very less and depends upon the counter cycle frequency.

Future Work

There is a scope for elimination of girth 4 which degrades the performance by constructing (Square matrix of redundant bit size, path of the parity check matrix) matrix in such a way that diagonal elements are not compulsory one's, without deviating involutive concept. Overlap between two columns is not greater than one is another constraint.

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